PLUS

10629672_CLSTITLES.txt
Titles of Most Frequently Occurring Classifications of Patents Returned
From A Search of 10629672 on November 03, 2005

28 365/201 (15 OR, 13 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/201 .Testing

10 714/718 (0 OR, 10 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/718 .Memory testing

7 365/185.23 (2 OR, 5 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/185.01 FLOATING GATE
365/185.18 .Particular biasing
365/185.23 ..Drive circuitry (e.g., word line driver)

7 365/200 (5 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/200 .Bad bit

6 365/230.03 (0 OR, 6 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/230.01 ADDRESSING
365/230.03 .Plural blocks or banks

6 365/230.06 (2 OR, 4 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/230.01 ADDRESSING
365/230.06 .Particular decoder or driver circuit

5 365/203 (1 OR, 4 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/203 .Precharge

5 714/719 (2 OR, 3 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/718 .Memory testing
714/719 ..Read-in with read-out and compare

4 365/189.04 (0 OR, 4 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/189.04 .Simultaneous operations (e.g., read/write)

4 365/189.05 (0 OR, 4 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/189.05 .Having particular data buffer or latch

3 365/185.04 (1 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/185.01 FLOATING GATE
365/185.04 .Data security

3 365/185.2 (0 OR, 3 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/185.01 FLOATING GATE
365/185.18 .Particular biasing
365/185.2 ..Reference signal (e.g., dummy cell)

3 365/189.07 (0 OR, 3 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/189.07 .Including signal comparison

3 365/210 (0 OR, 3 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/206 .Noise suppression
365/207 ..Differential sensing
365/209 ...Magnetic
365/210 ....Reference or dummy element

3 365/233 (2 OR, 1 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/230.01 ADDRESSING
365/233 .Sync/clocking

3 714/720 (0 OR, 3 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/718 .Memory testing
714/719 ..Read-in with read-out and compare
714/720 ...Special test pattern (e.g., checkerboard, walking ones)

2 365/185.21 (0 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/185.01 FLOATING GATE
365/185.18 .Particular biasing
365/185.2 ..Reference signal (e.g., dummy cell)
365/185.21 ...Sensing circuitry (e.g., current mirror)

2 365/189.01 (0 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT

2 365/189.03 (0 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/189.03 .Plural use of terminal

2 365/189.08 (0 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/189.08 .Including specified plural element logic arrangement

2 365/230.08 (0 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/230.01 ADDRESSING
365/230.08 .Including particular address buffer or latch circuit arrangement

2 365/238.5 (1 OR, 1 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL

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        365/230.01    ADDRESSING
        365/238.5     .Byte or page addressing

2  714/731       (1 OR, 1 XR)
        Class   714 :  ERROR DETECTION/CORRECTION AND FAULT
                         DETECTION/RECOVERY
        714/699       PULSE OR DATA ERROR HANDLING
        714/724       .Digital logic testing
        714/726       ..Scan path testing (e.g., level sensitive scan
                         design (LSSD))
        714/731       ...Clock or synchronization

2  714/736       (1 OR, 1 XR)
        Class   714 :  ERROR DETECTION/CORRECTION AND FAULT
                         DETECTION/RECOVERY
        714/699       PULSE OR DATA ERROR HANDLING
        714/724       .Digital logic testing
        714/736       ..Device response compared to expected
                         fault-free response

2  714/743       (1 OR, 1 XR)
        Class   714 :  ERROR DETECTION/CORRECTION AND FAULT
                         DETECTION/RECOVERY
        714/699       PULSE OR DATA ERROR HANDLING
        714/724       .Digital logic testing
        714/738       ..Including test pattern generator
        714/743       ...Addressing

2  714/744       (1 OR, 1 XR)
        Class   714 :  ERROR DETECTION/CORRECTION AND FAULT
                         DETECTION/RECOVERY
        714/699       PULSE OR DATA ERROR HANDLING
        714/724       .Digital logic testing
        714/738       ..Including test pattern generator
        714/744       ...Clock or synchronization
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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	178	test mode controller$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:54
L2	150	test mode setting signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:55
L4	89574	mode register set signal or (MRS)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:55
L5	760613	TMS	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:55
L6	760749	l5 or l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:56
L7	64222	address signal$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:56
L8	6138	l4 and l6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:56
L9	182	l7 and l8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:56

L10	1	l1 and l9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:57
L11	116	test mode decoder$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:58
L12	616	upper address bit$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:58
L13	496	lower address bit$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:58
L14	5	test mode item$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 12:59
L15	2	test mode item selecting	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:02
L16	2	l14 and l15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:00
L17	2	l11 and (l12 or l13)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:00

L18	2	l16 and l17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:00
L19	1	l18 and l9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:00
L20	5	l14 or l15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:00
L21	294	l11 or l9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:01
L22	2	l21 and (l14 or l15)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:02
L23	2003	test mode select$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:03
L24	1	l22 and l23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:03
L25	68	l21 and l23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:04

L26	68	l25 and (l12 or l13 or l4 or l6 or l14 or l11)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:07
L27	1	predetermined test mode item group	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:08
L28	2910	pull-up same output terminal$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:08
L29	1785	pull-down same output terminal$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:10
L30	1	l16 and (l27 or l28)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:10
L32	1	l26 and (l27 or l28)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:10
L33	42461	pull-down or pull-up	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:10
L34	22	l33 and l26	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:10

L35	11268	714/724 or 714/718 or 365/201 or 365/241 or 365/189.11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:19
L36	24315	address decoder$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:21
L37	3733401	(controller$1 or selector$1 or voter$1 or switch or MU or multiplex$3 or decision circuit$1or majority decision)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:23
L38	11410	714/797 or l35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:24
L39	17693	l36 and l37	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:24
L40	2	l39 and l34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:24
L41	22	l37 and l34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 14:08
L42	2	l38 and l41	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/11/03 13:25